Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] 1. A method for identifying and preventing logic errors in an integrated circuit caused by gate oxide leakage, comprising:

locating and compiling every net, which is an interconnect between a driving circuit and a receiving circuit, in an integrated circuit;

determining, for each receiving circuit, the gate area of each current sink transistor device;

determining, for each receiving circuit, the entire current source to current sink resistive interconnect network;

determining, for each driving circuit, the weakest pull-up circuit and the weakest pull-down circuit and converting them to equivalent resistances;

defining and modeling, for each net, a comprehensive DC resistance network of the driving circuit resistance, the interconnect resistance, and the current source resistance;

determining, for each sink transistor gate, the net pulled up and net pulled down to determine a DC solution of the gate voltage offset at each sink transistor gate;

determining any failing gates with a reference level voltage check of the gate voltage offset relative to a given

threshold;

using a static noise analysis tool to combine the determined gate voltage offset as a noise source with other noise sources, and performing a sensitivity analysis to determine the effect of the noise on the function on each receiving circuit gate;

redesigning each failed net.

[c2] 2. The method of claim 1, wherein the step of compiling includes compiling a list of nets in an integrated circuit in a chip or within a macro.

[c3] 3. The method of claim 1, wherein the step of determining the gate area of each current sink transistor device includes determining the actual device dimensions of each current sink transistor.

[c4] 4. The method of claim 1, wherein the step of determining the gate area of each current sink transistor device includes determining a gate capacitance load on each current sink transistor device, and converting the gate capacitance load to a current sink or current source relative to the size of the input capacitance.

[c5] 5. The method of claim 1, wherein the step of identifying failing gates uses an offset exceeding a given percentage of power supply voltage.

[c6] 6. The method of claim 1, wherein the step of identifying failing gates uses an offset exceeding a given percentage of power supply voltage, and the limit for any net is at least the unity gain point of the current sink gate.

[c7] 7. The method of claim 6, wherein the step of redesigning failed nets includes redesigning each failed net through electrical and logical optimization, including providing a wiring interconnect with a lower resistance, or a larger driver, or a smaller fanout, or by inserting additional buffers.

[c8] 8. The method of claim 1, wherein the step of defining and modeling, for each net, a comprehensive DC resistance network includes, for improved modeling in the DC network, an interconnect resistance parameter for each sink transistor that is measured from an input pin to the current source gate.

[c9] 9. The method of claim 1, wherein the step of determining, for each sink transistor gate, the net pulled up and net pulled down includes simulating a transition for each pull-up and pull-down network to determine a DC solution of the gate voltage offset at each sink gate for each simulated transition.

[c10] 10. The method of claim 1, where in the step of deter-

mining any failing gates with a reference level voltage check, a passing value corresponds to at least a unity gain of a sink gate.

[c11] 11. A method for identifying and preventing logic errors in an integrated circuit caused by gate oxide leakage, comprising:

defining every net, which is an interconnect between a driving circuit and a receiving circuit, in an integrated circuit;

determining, for each receiving circuit, the gate area of each current sink transistor device;

determining, for each receiving circuit, the entire current source to current sink resistive interconnect network;

determining, for each driving circuit, the weakest pull-up circuit and the weakest pull-down circuit and converting them to equivalent resistances;

defining a model, for each net, of a comprehensive DC resistance network of the driving circuit resistance, the interconnect resistance, and the current source resistance;

determining, for each sink transistor gate, the net pulled up and net pulled down to determine a DC solution of the gate voltage offset at each sink transistor gate;

determining any failing gates with a reference level voltage check of the gate voltage offset relative to a given

threshold;

combining the determined gate voltage offset as a noise source with other noise sources while performing a sensitivity analysis to determine the effect of the noise on the function on each receiving circuit gate;

redesigning each failed net.

[c12] 12. The method of claim 11, wherein the step of compiling includes compiling a list of nets in an integrated circuit in a chip or within a macro.

[c13] 13. The method of claim 11, wherein the step of determining the gate area of each current sink transistor device includes determining the actual device dimensions of each current sink transistor.

[c14] 14. The method of claim 11, wherein the step of determining the gate area of each current sink transistor device includes determining a gate capacitance load on each current sink transistor device, and converting the gate capacitance load to a current sink or current source relative to the size of the input capacitance.

[c15] 15. The method of claim 11, wherein the step of identifying failing gates uses an offset exceeding a given percentage of power supply voltage.

[c16] 16. The method of claim 11, wherein the step of identi-

fying failing gates uses an offset exceeding a given percentage of power supply voltage, and the limit for any net is at least the unity gain point of the current sink gate.

[c17] 17. The method of claim 16, wherein the step of redesigning failed nets includes redesigning each failed net through electrical and logical optimization, including providing a wiring interconnect with a lower resistance, or a larger driver, or a smaller fanout, or by inserting additional buffers.

[c18] 18. The method of claim 11, wherein the step of defining and modeling, for each net, a comprehensive DC resistance network includes, for improved modeling in the DC network, an interconnect resistance parameter for each sink transistor that is measured from an input pin to the current source gate.

[c19] 19. The method of claim 11, wherein the step of determining, for each sink transistor gate, the net pulled up and net pulled down includes simulating a transition for each pull-up and pull-down network to determine a DC solution of the gate voltage offset at each sink gate for each simulated transition.

[c20] 20. The method of claim 11, where in the step of deter-

mining any failing gates with a reference level voltage check, a passing value corresponds to at least a unity gain of a sink gate.